REMARKS

Claims 1, 3, 5 and 6 are pending in this application. Claim 3 has been amended and claim 9 has been canceled herein without prejudice or disclaimer.

Entry of this amendment is proper under 37 C.F.R. § 1.116 as the amendments:

(a) do not raise any new issue that would require further consideration and/or search (as the amendment merely incorporates the subject matter of claim 9 into claim 3);

(b) do not add any additional claims without canceling a corresponding number of claims;

(c) place the application in better form for appeal, should an appeal be necessary, by reducing the number of issues on appeal by incorporating claim 9 into claim 3. The amendments are necessary and were not earlier presented as they are in response to arguments raised in the final rejection. Entry of the Amendment is respectfully requested.

Claim Rejection – 35 USC § 102 and 35 USC § 103

Claims 1 and 5 were rejected under 35 U.S.C. 102(b) over Ohta et al. (EP 0493116). Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites, *inter-alia*, "A dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands mutually defined by a dielectrically separating oxide film on a surface of the wafer..." Claim 5 recites, *inter-alia*, "A diellectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands insulated by a dielectrically separating oxide film on the wafer surface, the diellectrically separated wafer comprises a surface between one diellectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat."

It is respectfully submitted that the grinding method of Ohta et al. cannot prevent the formation of an indentation 16a and a projection 16b having a step of approximately 0.3 μm or larger in a border of polysilicon layer 16 of Ohta et al. Applicants submit that the grinding method of Ohta et al. is conventional and most likely uses a grinding wheel having grinding abrasives thereon, such as a diamond powder. When a surface of a single crystal silicon is ground according to a conventional grinding method, there may be a problem in that a

grinding mark may be left on the surface of a single crystal silicon. Furthermore, the use of a grinding wheel has drawbacks. For example, the grinding wheel may be crushed when the grinding wheel gets in contact with an oxide layer. Consequently, the grinding method of Ohta et al. cannot achieve a flatness less than 0.2 μm.

In order to circumvent the above problems, a single crystal silicon wafer (10) is ground to only a certain extent and the surface is finished by a polishing method (see, for example, page 27, lines 22-26 in the specification). In this way, the present invention achieves a surface flatness of less than 0.2 μm.

Consequently, Ohta et al. does not disclose, teach or suggest the subject matter recited in claims 1 and 5.

Therefore, the Applicants respectfully submit that claim 1 and claim 5 are patentable and request that the §102 rejection of claims 1 and 5 be withdrawn.

Claim 3 was rejected under 35 U.S.C. 102(b) over Katayama (JP 02-52452).

Claim 3 has been amended to further recite "when the surface is measured by a stylus-profilometer, a flatness of the dielectrically separated silicon wafer is less than 0.2 μm as the absolute roughness between a maximum height and a minimum height."

The substrate 2 of Katayama is polished from a bottom face 2b and is removed flatwise down to a position 10 indicated by a one-dotted chain line. Similarly, the main surface 2a of the semiconductor substrate 2 is polished and removed flatwise down to a position 10 indicated by a one-dotted chain line. However, it is respectfully submitted that the term "polishing" as used in Katayama et al. merely refers to "grinding" because this operation is performed so as to remove the semiconductor substrate flatwise down to a position 10 indicated by a one-dotted chain line. Thus, the grinding operation of Katayama et al. is different from the polishing operation of the present invention. Thus, Katayama et al.'s grinding operation would not achieve a surface flatness of less than 0.2 μm.

Consequently, Katayama does not disclose, teach or suggest a flatness of the dielectrically separated silicon wafer is less than 0.2 μm as the absolute roughness between a maximum height and a minimum height, as recited in claim 3.

Therefore, Applicants respectfully submit that claim 3 is patentable and respectfully request that the §102 (b) rejection of claim 3 be withdrawn.

Claim 6 was rejected under 35 U.S.C. 102(b), or in the alternative, under 35 U.S.C. 103(a) as obvious over Ohta et al. Applicants traverse this rejection for at least the following reasons.

The Office Action contends that Ohta et al. teach the device of claim 5. The Office Action admits however that Ohta et al. did not expressly disclose that a flatness on the surface of the dielectrically separated islands is less than 0.2 μm when measured by a stylus-profilometer. The Examiner contends that this limitation is considered taught or obvious over Ohta et al. because the grinding will inherently create a surface having no difference between the maximum and minimum values of flatness or that it is considered within one of skill in the art to minimize any surface roughness as motivated by the relationship between the surface roughness and complications in processing. Applicants respectfully disagree.

The grinding method of Ohta et al. cannot prevent the occurrence of an indentation 16a and a projection 16b having a step of approximately 0.3 μm or greater in a border of polysilicon layers 16.

Moreover, Ohta et al. teaches that it is sufficient for a surface of a polycrystalline silicon layer 8 to be finished flat and smooth (in lines 58 of column 5 to line 9 of column 6). However, with regard to limitations in the grinding operation, Ohta et al. merely teaches that the thickness of the polycrystalline silicon layer 8 to be removed by grinding operation is desired to be approximately in the range of 30 to 60 μm such that the warpage of the substrate will be kept in the range of 0 to 80 μm. Furthermore, as stated above, with regard to claim 1 and 5, the conventional grinding method has drawbacks which do not allow achieving a surface flatness of 0.2μm or less.

In contrast, the present invention provides the manufacture of a dielectrically separated wafer without causing a defect pattern due to the adhesion of a resist, circuit connection, bad resolution, and removal of a mask only under conditions that a step in the indentation 16a and a projection 16b are approximately 0.2μm or smaller. Moreover, in order to achieve such a preferable dimension in the steps in the indentation 16a and the projection 16b, preferable conditions which are based on factors such as amount of polishing L1 (μm) and thickness of dielectrically separating oxide film (μm) are finally found by testing various conditions shown in TABLES 1 to 4 of the present application. The accuracy such as ± 0.2 μm achieved in the present invention differs from the limitations 30 to 60 μm taught by Ohta et al. In fact, Ohta et al. teaches away from a surface flatness of 0.2 μm or less as Ohta et al.

specifically teaches grinding the polycrystalline silicon layer to a surface flatness in the range of 30 to 60 μm.

Consequently, for at least the above reasons, Applicants submit that Ohta et al. does not disclose, teach or suggest the subject matter recited in claim 6.

Therefore, Applicants respectfully submit that claim 6 is patentable and respectfully request that the §102 and §103 rejections of claim 6 be withdrawn.

Claim 9 was rejected under 35 U.S.C. § 102(b), or in the alternative, under 35 U.S.C. § 103(a) as obvious over Katayama et al.

Claim 9 has been canceled without prejudice or disclaimer. Therefore, the rejections of claim 9 under § 102(b) and § 103(a) is rendered moot.

Therefore, Applicants respectfully request that the §102 and §103 rejections of claim 9 be withdrawn.

CONCLUSION

In view of the foregoing, the claims are now in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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